CLAIMS

1. A programmable memory on an inkjet printhead chip, the memory comprising:

a memory array having a plurality of memory elements; and

a bipolar device isolating a memory element from another memory element in the memory array.

2. The programmable memory of claim 1, wherein the memory element comprises a fuse element.

3. The programmable memory of claim 2, wherein the fuse element comprises at least one of tantalum aluminum, and tantalum aluminum nitride.

4. The programmable memory of claim 1, further comprising a plurality of layered heaters.

5. The programmable memory of claim 1, wherein the memory element comprises a floating gate element.

6. The programmable memory of claim 1, wherein the bipolar device comprises a pnp device.

7. The programmable memory of claim 6, further comprising a surrounding guard ring configured to isolate one pnp device from another pnp device.

8. The programmable memory of claim 7, wherein the surrounding guard ring comprises a p-type guard ring positioned around each pnp device.

9. The programmable memory of claim 7, wherein the surrounding guard ring comprises an n-type guard ring coupled to a high potential.

10. The programmable memory of claim 7, wherein the memory element is positioned within the surrounding guard ring.

11. The programmable memory of claim 7, wherein the memory element is positioned outside the surrounding guard ring.

12. The programmable memory of claim 6, wherein the memory array comprises rows and columns, wherein each pnp device has an n-type base, and wherein the pnp devices on each row are joined at the n-type base.

13. The programmable memory of claim 6, wherein the pnp devices are arranged in a plurality of rows and columns intersecting each other, and wherein the pnp devices on a row are isolated from the pnp devices of another row by a grounded p-type region.

14. The programmable memory of claim 6, wherein the pnp devices are arranged in a plurality of rows and columns intersecting each other, and wherein the pnp devices on a row are isolated from the pnp devices of another row by a high potential n-type region.

15. The programmable memory of claim 1, wherein the bipolar device comprises a npn device.

16. The programmable memory of claim 1, wherein the bipolar device comprises a diode.

17. The programmable memory of claim 1, further comprising a memory density comprising a sum of areas occupied by the memory element and a programming transistor, the memory density is at least 200 bits per square millimeter.

18. The programmable memory of claim 1, wherein the memory has at least 128 memory elements, and each memory element has a resistance of at least 5 ohms on the inkjet printhead chip.

19. A programmable memory on an inkjet printhead chip, the memory comprising:

a memory array having a plurality of circuit elements arranged in rows and a plurality of circuit elements arranged in columns intersecting the rows to thereby form a plurality of memory elements; and

a biplolar element coupled to the memory element and configured to isolate the memory element from another memory element.

20. The programmable memory of claim 19, wherein the fuse element comprises at least one of tantalum aluminum, and tantalum aluminum nitride.

21. The programmable memory of claim 19, further comprising a plurality of layered heaters.

22. The programmable memory of claim 19, wherein the circuit element comprises a pnp device.

23. The programmable memory of claim 19, further comprising a surrounding guard ring configured to the circuit element from another circuit element.

24. The programmable memory of claim 23, wherein the surrounding guard ring comprises a p-type guard ring positioned around each circuit element.

25. The programmable memory of claim 23, wherein the surrounding guard ring comprises an n-type guard ring coupled to a high potential.

26. The programmable memory of claim 23, wherein the fuse element is positioned within the surrounding guard ring.

27. The programmable memory of claim 23, wherein the fuse element is positioned outside the surrounding guard ring.

28. The programmable memory of claim 22, wherein each pnp device has an n-type base, and wherein the circuit elements on each row are joined at an n-type base

29. The programmable memory of claim 22, wherein the pnp devices on a row are isolated from the pnp devices of another row by a grounded p-type region.

30. The programmable memory of claim 22, and wherein the pnp devices on a row are isolated from the pnp devices of another row by a high potential n-type region.

31. The programmable memory of claim 19, wherein the circuit element comprises a npn device.

32. The programmable memory of claim 19, wherein the circuit element further comprises a plurality of layered heaters.

33. The programmable memory of claim 19, further comprising a memory density comprising a sum of areas occupied by the memory element and a programming transistor, the fuse density is at least 200 bits per square millimeter.

34. The programmable memory of claim 19, wherein the memory has at least 128 memory elements, and each memory element has a resistance of at least 5 ohms on the inkjet printhead chip.

35. A method of providing high fuse density in a printhead heater chip, the method comprising:

arranging a plurality of memory elements in a memory array; and

isolating a memory element from another memory element in the memory array with a bipolar device.

36. The method of claim 35, wherein the memory element comprises a fuse element.

37. The method of claim 36, wherein the fuse element comprises at least one of tantalum aluminum, and tantalum aluminum nitride.

38. The method of claim 35, further comprising providing a plurality of layered heaters on the heater chip.

39. The method of claim 35, wherein the memory element comprises a floating gate element.

40. The method of claim 35, wherein the bipolar device comprises a pnp device.

41. The method of claim 40, further comprising isolating the pnp device with a surrounding guard ring.

42. The method of claim 40, wherein the surrounding guard ring comprises a p-type guard ring, further comprising positioning the p-type guard ring around each pnp device.

43. The method of claim 40, wherein the surrounding guard ring comprises an n-type guard ring, further comprising coupling the n-type guard ring to a high potential.

44. The method of claim 40, further comprising positioning the memory element within the surrounding guard ring.

45. The method of claim 40, further comprising positioning the memory element outside the surrounding guard ring.

46. The method of claim 40, wherein the memory array comprises rows and columns, and each pnp device has an n-type base, further comprising joining the pnp devices on each row at the n-type base.

47. The method of claim 40, further comprising:

arranging the pnp devices in a plurality of rows and columns intersecting each other; and

isolating the pnp devices on a row from the pnp devices of another row by a grounded p-type region.

48. The method of claim 40, further comprising:

arranging the pnp devices in a plurality of rows and columns intersecting each other; and

isolating the pnp devices on a row from the pnp devices of another row by a high potential n-type region.

49. The method of claim 35, wherein the bipolar device comprises a npn device.

50. The method of claim 35, wherein the bipolar device comprises a diode.

51. The method of claim 35, further comprising providing at least 200 bits per square millimeter including a sum of areas occupied by the memory element and a programming transistor.

52. The method of claim 35, further comprising providing at least 128 memory elements, and each memory element having a resistance of at least 5 ohms on the inkjet printhead chip.

53. A programmable memory on an inkjet printhead chip, the memory comprising:

a memory array having a plurality of memory elements and at least one programming transistor, and having a memory density comprising a sum of areas occupied by the memory elements and the programming transistor, and wherein the memory density is at least 200 bits per square millimeter.

54. A programmable memory on an inkjet printhead chip, the memory comprising:

a memory array having a plurality of at least 128 memory elements, and wherein each memory element has a resistance of at least 5 ohms on the inkjet printhead chip.